

Appl. No. : 10/008,408  
Filed : November 13, 2001

REMARKS

In the Office Action, the examiner objected to Claims 2, 4 and 6 on the ground that the plurality of elements are not separated by a line indentation. Further, the examiner objected to Claim 6 on the ground that the term "overall" renders the claim indefinite. Accordingly, the applicant has amended the claims to correct the informalities.

The examiner rejected Claims 1 and 5 under 35 U.S.C. 102(b) as being anticipated by Huston et al. (U.S. Patent No. 6,079,038). The cited Huston et al. reference discloses a method of operating an integrated circuit tester which includes a process of producing a Shmoo plot contour graph. The examiner rejected Claims 2, 3, 4 and 6 under 35 U.S.C. 103(a) as being obvious over the technology disclosed by the cited Huston et al. reference noted above in view of Ullmann (U.S. Patent No. 5,731,984).

Accordingly, the applicant has amended the set of claims to more clearly define the feature of the present invention. More precisely, the applicant has amended Claim 1 to include the limitation that "the test parameters and the test result data are illustrated in a three-dimensional manner on X, Y and Z axes", which is not shown or suggested by the cited Huston et al. reference or the cited Ullmann reference.

The present application describes a method and system to obtain and display response from an Integrated Circuit (IC) device

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under test when an IC device is being tested by an event tester rather than a conventional cycle base tester. In the event tester, the test patterns which are timed event data are used. The event data is different from test pattern data that are divided by each test cycle used in the cycle base tester. In the cycle base tester, the test patterns are signal waveforms that are analog in nature. It should be noted that the response from the IC device tested by the event tester is also very different from that of the IC device tested by the cycle base tester.

Because the data applied (test patterns) and data received (response) from IC are of different nature in two test systems, the conventional methods to display received data cannot be used. For example, as mentioned above, the scaling of checkerboard means scaling of time difference between events. This scaling should not be confused with the waveform expansion as described in the cited Ullmann reference, or as it is done by the conventional instruments such as oscilloscope. There is no notion of events in the cited Ullmann reference or in conventional instruments such as oscilloscope. When the notion of events itself is not present, one cannot envision scaling of event timing in the presence of the cited references and conventional instruments.

As event tester uses event and their timing to define test data (test patterns), and specifies this test data for each pin independently (no cyclization), the characterization map becomes pin failures with respect to time. As there is no notion of event

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timing, the applicant believes this cannot be done in the conventional methods. Indeed, there is no notion of pin failure with respect to time in any of the cited references.

The true nature of a transition in a signal is of analog nature, conventional instruments such as oscilloscope capture that behavior. The event tester uses events that are 0-to-1 and 1-to-0 transitions, hence, the analog information in the signal during the transition itself is lost. The benefit of event tester is that it uses timed event data; therefore, if an error occurs, it can be quickly checked in the electronic design automation (EDA) environment of IC design such as Verilog and VHDL.

As discussed above, none of the cited references show the three-dimensional views of the present invention for displaying various parameters involved in testing the IC device. Further, none of the cite references show the notion of event or event timing. Therefore, the present invention is not anticipated by Huston et al. or obvious over the technologies disclosed by the cited references taken singly or in combination. Accordingly, the applicant believes that the rejections under 35 U.S.C. 102(b) and 103(a) are no longer applicable to the present application.

In this opportunity, the applicant has amended the specification to correct the minor errors therein and to more clearly disclose the present invention. This is to verify that no new matter has been introduced by this amendment.


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In view of the foregoing, the applicant believes that Claims 1-6 are in condition for allowance, and accordingly, Applicant respectfully requests that the present application be allowed and passed to issue.

Respectfully submitted,

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